REMARKS/ARGUMENTS

STATUS OF CLAIMS

In response to the Office Action dated August 9, 2007, claims 2, 3, 6 and 9 have been amended, and claim 8 has been canceled. Claims 1-7 and 9 are now pending in this application. No new matter has been added.

The indication that claim 7 is allowable and that claim 3 is objected to, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims, is acknowledged and appreciated.

By this response, claim 3 has been amended to be in independent form including all the limitations of claims 1 and 2. Consequently, claim 3, as amended, is believed to be allowable.

Claims 2 and 6 have been amended to begin with "The" instead of "A". The claim amendments are non-narrowing claim amendments.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claims 8 and 9 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Since claims 8 and 9 include "a signal timing adjustment device", the Examiner contends that it is unclear whether the claims are directed to a program or device (claim 8), or a computer-readable medium or device (claim 9).

The rejection is moot as to canceled claim 8, and claim 9 has been amended to change "a signal timing adjustment device" to "a signal timing adjustment section". Therefore, amended

claim 9 recites the invention with the degree of precision and particularity required by the statute. Therefore, it is respectfully urged that the rejection be withdrawn.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 101

Claims 8 has been rejected under 35 U.S.C. §101, as being directed to non-statutory subject matter. The Examiner contends that the claim is directed to "software per se" since it is directed to "A signal timing adjustment amount setting program..."

The rejection is moot as to canceled claim 8.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 103

Claims 1, 2 and 4-6 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto et al. (USPN 6,424,184) in view of Yamada (USPN 5,912,591), relied upon by the Examiner as disclosing a delay circuit that applies back biases to a transistor to raise the threshold of the transistor and increase the delay time.

The rejections are respectfully traversed.

Independent claim 1 recites, *inter alia*:

> ...***an adjustment voltage*** that is in accordance with a delay-time adjustment amount, which ***is set so that delay time of each circuit block in an integrated circuit becomes closer to an average value of the delay time***, the delay time being time between an input of data to the circuit block and an output of the data from the circuit block; and
>
> a delay-adjustment section for increasing or decreasing the delay time by using a transistor at which a threshold voltage changes in accordance with a value of the adjustment voltage selected.

The Examiner maintains that adjustment voltage is disclosed in Tamamoto et al. at column 1, lines 42-44 which describe:

> Still another objective of the present invention is to provide a method for adjusting an input and output characteristic of the frequency-voltage conversion circuit of the system.

While input and output characteristics of the frequency-voltage conversion circuit of the system may be adjusted, there is no description at column 1, lines 42-44 of Tamamoto et al. that the adjustment voltage is set so that delay time of [each] circuit block in an integrated circuit ***becomes closer to an average value of the delay time***. This is what is disclosed in the present application, not in Tamamoto et al. or Yamada.

It should be noted that it is well recognized in patent law that it is impermissible to simply engage in hindsight reconstruction of the claimed invention, using Applicants' disclosure to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103. The present rejection is an example of improper application of hindsight considerations to reject the claims.

Furthermore, the voltage selecting section and the delay-adjustment section of claim 1 of the present application are to adjust delay time. Claim 1 clearly delineates delay time is time between an input of data to each of a plurality of circuit blocks in an integrated circuit and an output of the data therefrom. Hence, the input and output characteristic of each circuit block of the integrated circuit is adjusted.

In the integrated circuit in the initial state, the delay time of each circuit block is significantly different from one another. Even if an average value of an operation frequency of each circuit block is high, a circuit block, which operates at a lowest speed (whose delay time is the longest), determines the operation frequency (specification value) of the integrated circuit.

In view of this, the voltage selecting section and the delay-adjustment section are used to set the delay time of each circuit block to be close to the average value. As a result, the operating frequency (specification value) of the integrated circuit becomes higher than the value before the adjustment (see specification, page.31, lines 8-23, and Fig. 12).

In contrast, Yamamoto, column 1, lines 42-44 describe, "Still another objective of the present invention is to provide a method for adjusting an input and output characteristic of the frequency-voltage conversion circuit of the system". In Yamamoto, the system includes a frequency-voltage conversion circuit for supplying a minimum operating voltage required for the target circuit to normally operate (see Yamamoto, column 1, lines 38-41).

That is, the input and output characteristic of the target circuit is **NOT** adjusted, but the input and output characteristic of the frequency-voltage conversion circuit for supplying the operating voltage to the target circuit is adjusted. As such, the system of Yamamoto is fundamentally different from the present invention in which the input and output characteristic of each circuit block of the integrated circuit is adjusted.

Further, the frequency-voltage conversion circuit of Yamamoto is to find the minimum operating voltage required for the target circuit to normally operate. Such a frequency-voltage conversion circuit is fundamentally different from the signal timing adjustment of the present application, i.e., the signal timing adjustment sets the delay time of each circuit block of the integrated circuit to be close to the average value thereof. A person of ordinary skill in the art would never reasonably interpret adjusting the input and output characteristic of the frequency-voltage conversion circuit for supplying the operating voltage to the target circuit, disclosed in Yamamoto, as being the same as setting the delay time of each circuit block in an integrated

circuit so that delay time becomes closer to an average value of the delay time, where delay time is required to be the time between an input of data to the circuit block and an output of the data from the circuit block.

In view of the above, it is respectfully submitted that the Examiner has not established a *prima facie* case of obviousness with regard to the claims 1, 2 and 4-6. Consequently, claims 1, 2 and 4-6 are patentable over Tamamoto et al. and Yamada and their allowance is respectfully solicited.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Edward J. Wise (Reg. No. 34,523) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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